M. Tech.(VLSI & Embedded System Design)
Programme Structure

Second Semester				
Sl. No.	**Course Code**	**Course Title**	**L-T-P**	**Credit**
1	VLM201	**Program Core - III** Analog and Digital CMOS VLSI Design	3-0-0	3
2	VLM202	**Program Core - IV** VLSI Design Verification and Testing	3-0-0	3
3	VLM231 VLM232 VLM233	**Program Elective - III** Memory Technologies SoC Design Low power VLSI Design	3-0-0	3
4	VLM241 VLM242 VLM243	**Program Elective - IV** Communication Buses and Interfaces/ Network Security and Cryptography/ Physical design automation	3-0-0	3
5	VLM205	Audit Course -2	2-0-0	0
6	VLM206	**Laboratory - III** Analog and Digital CMOS VLSI Design Lab	0-0-4	2
7	VLM207	**Laboratory - IV** VLSI Design Verification and Testing Lab	0-0-4	2
8	VLM208	Mini Project with Seminar	2-0-0	2
Total Credits				18

Audit course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

VLM201	Analog and Digital CMOS VLSI Design (3-0-0)	3 Credits

Module-1: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

Module-2: Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Module-3: Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc. Analog CMOS Design:

Module-4: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Commongate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Module-5: Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

Module-6: Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

Text Books:

1. J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.
3. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd Edition.

5. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
6. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

VLM202	VLSI Design Verification and Testing (3-0-0)	3 Credits

Module-1: Verification guidelines: Verification Process, Basic Testbench functionality, directedtesting, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

Module-2: Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

Module-3: Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Module-4: SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

Module-5: Randomization: Introduction, What to randomize, Randomization in SystemVerilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions,

Module-6: Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

Text Books:

1. Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
3. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design,Specification, and Verification Language).
4. System Verilog website – www.systemverilog.org
5. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
6. General reuse information and resources www.design-reuse.com
7. OVM, UVM(on top of SV) www.verificationacademy.com
8. Verification IP resources http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
9. http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/defa ult.aspx

VLM231	Memory Technologies (3-0-0)	3 Credits

Module-1: Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Module-2: DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

Module-3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Module-4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Module-5: Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Module-6: Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Edition
3. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI

VLM231	SoC Design (3-0-0)	3 Credits

Module-1:ASIC - Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Module-2: NISC - NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instructionset Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Module-3: Simulation - Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Module-4: Low power SoC design / Digital system, - Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Module-5: Synthesis - Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysisSingle core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

Module-6: Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Note: Students will prepare and present a term paper on relevant identified current topics (in batches of three students per topic) as a part of theory course.

Text Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
3. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
4. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
5. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

VLM233	Low Power Design (3-0-0)	3 Credits

Module-1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Module-2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Module-3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

Module-4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

Module-5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Module-6: Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

Text Books:

1. P Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.
3. J B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
4. A P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

VLM241	Communication Busses and Interfaces (3-0-0)	3 Credits

Module-1: Serial Busses - Physical interface, Data and Control signals, features,

Module-2: limitations and applications of RS232, RS485, I2 C, SPI

Module-3: CAN - Architecture, Data transmission, Layers, Frame formats, applications

Module-4: PCIe - Revisions, Configuration space, Hardware protocols, applications

Module-5: USB - Transfer types, enumeration, Descriptor types and contents, Device driver

Module-6: Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

Text Books:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

VLM242	Network Security and Cryptography (3-0-0)	3 Credits

Module-1: Security - Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Module-2: Number Theory - Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Module-3: Private-Key (Symmetric) Cryptography - Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Module-4: Public-Key (Asymmetric) Cryptography - RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Module-5: Authentication - IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Module-6: System Security - Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
3. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
4. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
5. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

VLM243	Physical Design Automation (3-0-0)	3 Credits

Module-1: Introduction to VLSI Physical Design Automation.

Module-2: Standard cell, Performance issues in circuit layout, delay models Layout styles.

Module-3: Discrete methods in global placement.

Module-4: Timing-driven placement. Global Routing Via Minimization.

Module-5: Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.

Module-6: Compaction, algorithms, Physical Design Automation of FPGAs..

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
3. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
4. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
5. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

VLM205	Audit Course (2-0-0)	0 Credit

VLM206	Analog and Digital CMOS VLSI Design Laboratory (0-0-4)	2 Credits

List of Experiments:

1. Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.

   a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.

   b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.

   c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.

   d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.

   e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV

   To extract Vth use the following procedure.

   i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
   ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
   iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.

   f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate your result according to technologies and comment on it.

2. Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.

   a) Perform the following

   i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.

   ii. Plot VTC for CMOS inverter with varying VDD.

   iii. Plot VTC for CMOS inverter with varying device ratio.

   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)

c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)

3. Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4. Perform the following

a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

   i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.

   ii. Calculate input bias voltage if bias current=50uA.

   iii. Use Ngspice and obtain the bias current. Compare its value with 50uA.

   iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

   v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW

   vi. Use Ngspice to determine input voltage range of the amplifier

5. Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA.

Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that
   a. low-frequency voltage gain = 5x104,
   b. unity gain BW (fu) = 500KHz,
   c. input capacitance=0.2pF,

d. output resistance = ,
e. CMRR=120dB

iv. Draw schematic diagram of CMRR simulation setup.

v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

6. Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.

a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.

d) Use interconnect length obtained and connect the second and third inverter. Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part 'c'.

VLM208	VLSI Design Verification and Testing Laboratory (0-0-4)	2 Credits

List of Experiments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool chain

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

Audit Courses 1 & 2: English for Research Paper Writing

Course objectives:

Students will be able to:

1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Unit – I : **(4 Hours)**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit – II : **(4 Hours)**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

Unit – III : **(4 Hours)**

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit – IV : **(4 Hours)**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

Unit – V : **(4 Hours)**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

Unit – VI : **(4 Hours)**

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

Audit Courses 1 & 2: Disaster Management

Course Objectives: -

Students will be able to:

1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Unit – I : (4 Hours)

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

Unit – II : (4 Hours)

Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

Unit – III : (4 Hours)

Disaster Prone Areas In India: Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides and Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics

Unit – IV : (4 Hours)

Disaster Preparedness And Management : Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data rom Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Unit – V : (4 Hours)

Risk Assessment: Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global

Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.

Unit – VI : (4 Hours)

Disaster Mitigation: Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.

Suggested readings:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep &Deep Publication Pvt. Ltd., New Delhi.

Audit Courses 1 & 2: Sanskrit for Technical Knowledge

Course Objectives:

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects
4. enhancing the memory power
5. The engineering scholars equipped with Sanskrit will be able to explore the
6. huge knowledge from ancient literature

Unit – I : (8 Hours)

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences.

Unit – II : (8 Hours)

Order, Introduction of roots, Technical information about Sanskrit Literature.

Unit – III : (8 Hours)

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics.

Course Outcome:

Students will be able to

1. Understanding basic Sanskrit language

2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

Suggested reading

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Audit Courses 1 & 2: Value Education

Course Objectives:

Students will be able to

1. Understand value of education and self- development
2. Imbibe good values in students
3. Let the should know about the importance of character

Unit – I : (4 Hours)

- Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism.

Unit – II : (6 Hours)

- Moral and non- moral valuation. Standards and principles.
- Value judgements
- Importance of cultivation of values.
- Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness.
- Honesty, Humanity. Power of faith, National Unity.
- Patriotism.Love for nature,Discipline

Unit – III : (6 Hours)

- Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline.
- Punctuality, Love and Kindness.
- Avoid fault Thinking.
- Free from anger, Dignity of labour.
- Universal brotherhood and religious tolerance.
- True friendship.
- Happiness Vs suffering, love for truth.
- Aware of self-destructive habits.
- Association and Cooperation.

- Doing best for saving nature

Unit – IV : **(6 Hours)**

- Character and Competence –Holy books vs Blind faith.
- Self-management and Good health.
- Science of reincarnation.
- Equality, Nonviolence,Humility, Role of Women.
- All religions and same message.
- Mind your Mind, Self-control.
- Honesty, Studying effectively

Course outcomes:
Students will be able to:

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

Suggested reading

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

Audit Courses 1 & 2: Constitution of India

Course Objectives:
Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Unit – I : **(4 Hours)**

History of Making of the Indian Constitution: History, Drafting Committee, (Composition & Working)

Unit – II : **(4 Hours)**

Philosophy of the Indian Constitution: Preamble Salient Features

Unit – III : **(4 Hours)**

Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Unit – IV : **(4 Hours)**

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions

Unit – V : **(4 Hours)**

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative CEO of Municipal Corporation.
Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy

Unit – VI : **(4 Hours)**

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Course Outcomes:
Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

Suggested reading:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.

3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Audit Courses 1 & 2: Pedagogy Studies

Course Objectives:
Students will be able to:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Unit – I : **(4 Hours)**

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

Unit – II : **(2 Hours)**

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit – III : **(4 Hours)**

Evidence on the effectiveness of pedagogical practices. Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Unit – IV : **(4 Hours)**

Professional development: alignment with classroom practices and follow-up support Peer support, Support from the head teacher and the community. Curriculum and assessment Barriers to learning: limited resources and large class sizes

Unit – V : **(2 Hours)**

Research gaps and future directions: Research design, Contexts. Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Course Outcomes:
Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what

conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Suggested Reading:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Audit Courses 1 & 2: Stress Management by Yoga

Course Objectives

1. To achieve overall health of body and mind
2. To overcome stress

Unit – I : **(4 Hours)**

Definitions of Eight parts of yog. (Ashtanga)

Unit – II : **(4 Hours)**

Yam and Niyam.

Do`s and Don't's in life.

(i) Ahinsa, satya, astheya, bramhacharya and aparigraha
(ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

Unit – III : **(4 Hours)**

Asan and Pranayam

(i) Various yog poses and their benefits for mind & body
(ii) Regularization of breathing techniques and its effects-Types of pranayam

Suggested Reading:

1. 'Yogic Asanas for Group Tarining-Part-I" :Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency.